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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/350,436	07/09/1999	CHANG-RAE JEONG	P992004	8102
33942	7590	06/10/2005	EXAMINER	
CHA & REITER, LLC 210 ROUTE 4 EAST STE 103 PARAMUS, NJ 07652			WANG, TED M	
			ART UNIT	PAPER NUMBER
			2634	

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

UK

Office Action Summary	Application No.	Applicant(s)	
	09/350,436	JEONG, CHANG-RAE	
	Examiner	Art Unit	
	Ted M. Wang	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 July 1999 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date. _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed on 11/12/2004, have been fully considered but they are not persuasive. The Examiner has thoroughly reviewed Applicants' arguments but firmly believes that the cited reference to reasonably and properly meet the claimed limitations.

Independent Claims 1 and 6

(1) *Applicants' argument* – Claim 1 requires, "Takahashi fails to show how "mixer" performs "selectively releasing and transmitting" of said input digital signal modulated by said one of said two different modulation standards and said converted input digital signal to the other one of said two different modulation standards by said codec means "occurs" in response to said channel select signal. The examiner is wrongly equate the mixers in the present invention with the encoding law conversion memory 24. The function of the mixers in the present invention is to operate in response to a mixing control signal for storing the digital signal that are output without any conversion operated thereon by the codec 210 (page 11, lines 16-20). Hence, the mixer is used in conjunction with the codec 210 to selectively convert specified channels."

Examiner's response -- In response to applicant's argument as recited in the above paragraph, the Takahashi reference discloses an encoding law conversion memory (Fig. 1-4 element 24) performs "selectively releasing and transmitting" (column 3 line 7- column 5 line 51) of said input digital signal modulated by said

one of said two different modulation standards (Fig.1 elements 13 and 14) and said converted input digital signal to the other one of said two different modulation standards (Fig.4 element 24) by said codec means "occurs" in response to said channel select signal (Fig.3 elements 34 and 29, column 3 line 41 – column 5 line 51, and Table 3). That is, the encoding law conversion memory receives either A-Law or u-Law modulated signal from secondary time switch (Fig.2 element 23) via digital trunks (Fig.1 elements 13 and 14) and in response to the selected signals or control signals generated by read address counter, selector, and control memory (Fig.3 elements 33, 34 and 29 and Table 3), it releases and transmits the non-encoded signal to A-Law or u-Law terminal (Fig.4 element 41 or 42) if $(M1, M0) = (0, 0)$ or $(1, 0)$ or converts the received signal to its appropriated signal and releases and transmits the encoded signal to A-Law or u-Law terminal (Fig.4 element 41 or 42) if $(M1, M0) = (0, 1)$ or $(1, 1)$. Clearly, the encoding law conversion memory 24 performs the equivalent functions of the CODEC and mixer as discloses by the instant applicant. Thus, for the explanation addressed in the above paragraph, the rejection under 35 U.S.C. 102(b) with Takahashi's reference is adequate.

(2) With regard claim 6, which recites the same above quoted argument, the explanation of all the argument is already addressed in the above paragraph.

Specification

2. The disclosure is objected to because of the following informalities:
 - On page 7 line 17, change "that" to --- there --- before "are".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Takahashi (US 4,661,946).

- In regard claim 1, Takahashi discloses a digital switch module having encoding law conversion capability for converting pulse code modulation (PCM) signals (column 1 lines 45-63, and column 3 lines 56-65) from either one of two different modulation standards to the other one of said two different modulation standards (Fig.1 elements 13 and 14) in a system characterized by having a plurality of communication channels with each channel having a plurality of input digital signals modulated by said one of said two different modulation standards (column 2 line 62 – column 3 line 19 and Fig.1 elements 10, 13, and 14) that comprise:

a channel selector for generating a channel select signal (Fig.3 elements 29, 32, and 34) for identifying said at least one channel of the multiple channels in said system (Fig.2 elements 26-31, Fig.3 elements 29, 32-34, and column 3 line 20 – column 5 line 51),

and at least one codec (Fig. 1-4 element 24) means for selectively converting said identified input digital signals received in said at least one channel from said one of said two different modulation standards to the other one of said two different modulation standards in response to said channel select signal (Fig. 1-4 elements 24 and 29, and column 2 line 62 – column 3 line 40),

a plurality of mixers for selectively releasing and transmitting (column 3 line 7- column 5 line 51) said input digital signal (Fig. 1-4 elements 24 and column 3 line 7 – column 6 line 39, where the mixers are considered as a device including a read only memory, ROM, which contains conversion data for converting between encoding laws with the control memory 29 that outputs control data from an address in the control memory 29 corresponding to each of the time slots to the ROM in response to the selected signal),

modulated by said one of said two different modulation standards (Fig. 1 elements 10, 13, and 14 and column 2 line 62 – column 3 line 19) and said converted input digital signal to the other one of said two different modulation standards by said codec means in response to said channel select signal (Fig. 1-4 elements 24 and 29, and column 2 line 62 – column 3 line 40, column 3 line 41 – column 5 line 51, and column 6 lines 1-46).

- In regard claim 2, the limitation is a conventional approaching that converting from one encoding law to the other is performed by converting the input data signal from the first encoding law to an analog signal and then re-encoding the analog signal according to the second encoding law. This process has difficulties

not found in an all-digital system and typically requires more expensive equipment than an all digital system. Therefore, it would be preferable to convert data signals from one encoding law to another without conversion to an analog signal. Further refer to Takahashi in column 1 lines 35-44.

- In regard claim 3, the limitation of a first buffer for receiving said converted input digital signal by said other one of said two different modulation standards from said codec means, and a second buffer sharing an output terminal with said first buffer for receiving said input digital signal modulated by said one of said two different modulation standards can further be taught in Fig. 3 elements 24 and 29, Fig.4 elements 24, 41, and 42, and column 41 – column 5 line 51, and column 6 lines 1-46.
- In regard claim 4, the limitation that channel select signal is generated in response to a frame sync signal, a clock signal, and a read address controlled by said clock signal for reading an output data or in response to each time slot can further be taught in Fig. 2 elements 20-31, and Fig.3 elements 24,29, 32-34, and 241, and column 2 lines 3-25, column 3 line 1 – column 5 line 51, and claim 6.
- In regard claim 5, all limitation can further be taught in Fig. 2 elements 20-31, and Fig.3 elements 24,29, 32-34, and 241, and column 2 lines 3-25, column 3 line 1 – column 5 line 51, and claim 6.
- In regard claim 6, all limitation is contained in claim 1 and 2. The explanation of all the limitation is already addressed in the above paragraph.

- In regard claim 7, all limitation is contained in claim 3. The explanation of all the limitation is already addressed in the above paragraph.
- In regard claim 8, all limitation is contained in claim 3. The explanation of all the limitation is already addressed in the above paragraph.
- In regard claim 9, all limitation is contained in claim 3. The explanation of all the limitation is already addressed in the above paragraph.
- In regard claim 10, all limitation is contained in claim 4. The explanation of all the limitation is already addressed in the above paragraph.
- In regard claim 11, all limitation is contained in claim 5. The explanation of all the limitation is already addressed in the above paragraph.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2634

Ted M. Wang



SHUWANG LIU
PRIMARY EXAMINER